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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,993	10/20/2003	Ok Byung Kim	1514.1031	1374

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STEIN, MCEWEN & BUI, LLP
1400 EYE STREET, NW
SUITE 300
WASHINGTON, DC 20005

EXAMINER	
RIELLEY, ELIZABETH A	

ART UNIT	PAPER NUMBER
2879	

DATE MAILED: 04/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/687,993	KIM ET AL.	
	Examiner	Art Unit	
	Elizabeth A. Rielley	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7,8,11 and 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7,8,11 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed 1/17/06 has been entered and considered by the Examiner. Claim 12 has been added. Currently, claims 1-5, 7, 8, 11, and 12 are pending in the instant application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 7, 8, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mitanaga et al (US 5923997) in view of Shimizu et al (US 6255146).

In regard to claim 1, Mitanaga et al ('997) teach a display device with a polysilicon substrate (250; figures 3b and 5a; column 13 line 47 to column 14 line 55), comprising: a display region (PTFT, 111, 133; figure 2; column 13 line 11-column 14 line 55) and a driving region (NTFT; figure 2; column 13 line 11 – column 14 line 55; claims 10-15); a first plurality of thin film transistors in the display region (PTFT; figure 2); a second plurality of thin film transistors (NTFT) and primary crystal grain boundaries (216; figure 5B;column 14 lines 55-65) in the polysilicon substrate in the display region and in the driving region (claim 10); secondary crystal grain boundaries in the polysilicon substrate in the display region and the driving region (claim 10 states that both active regions have at least one grain boundary, claims 13

and 14 teach that the TFTs are used for both a display region and a driver region); wherein the primary crystal grain boundaries are inclined to a first direction of current flowing from source (208) to drain (210) of each of the first plurality of thin film transistors at an angle of -30° to 30° (figure 5b; column 14 line 56 to column 15 line 4; claim 10, the grain boundaries of the first active region are parallel to the direction of current, thereby making that angle 0°); and wherein the primary crystal grain boundaries are inclined to a second direction of current flowing from source to drain of each of the second plurality of thin film transistors at an angle of 30° to 150° (claim 10; lines 47-column 16 line 17; claim 10 states that the crystal grain boundaries in the second region are perpendicular to the second current in the second TFT – the first current being in the first TFT – these primary crystal grain boundaries in the second region being perpendicular to the current would then be at an angle of 90°). Mitanaga et al ('997) are silent regarding the limitations of the secondary crystal grain boundaries are inclined to a second direction of current flowing from source to drain of each of the first plurality of thin film transistors, and the secondary crystal grain boundaries are inclined to the first direction of the current flowing from source to drain of each of the second plurality of thin film transistors. However, one skilled in the art would reasonably contemplate modifying the device of Mitanaga et al ('997) to include the claimed secondary crystal grain boundaries are inclined to a second direction of current flowing from source to drain of each of the first plurality of thin film transistors, and the secondary crystal grain boundaries are inclined to the first direction of the current flowing from source to drain of each of the second plurality of thin film transistors, as an obvious matter of design engineering as evidenced by Shimizu et al ('146). Shimizu et al teach crystal grain boundaries perpendicular to other crystal grain boundaries in many different ways, and Shimizu does not make a distinction between primary and secondary boundaries (column 1 lines 21-42; column 12 line 35 to column 13 line 4). Therefore figure 44 as described below teaches the claimed secondary boundaries (arrows indicate current flow).

FIG.44

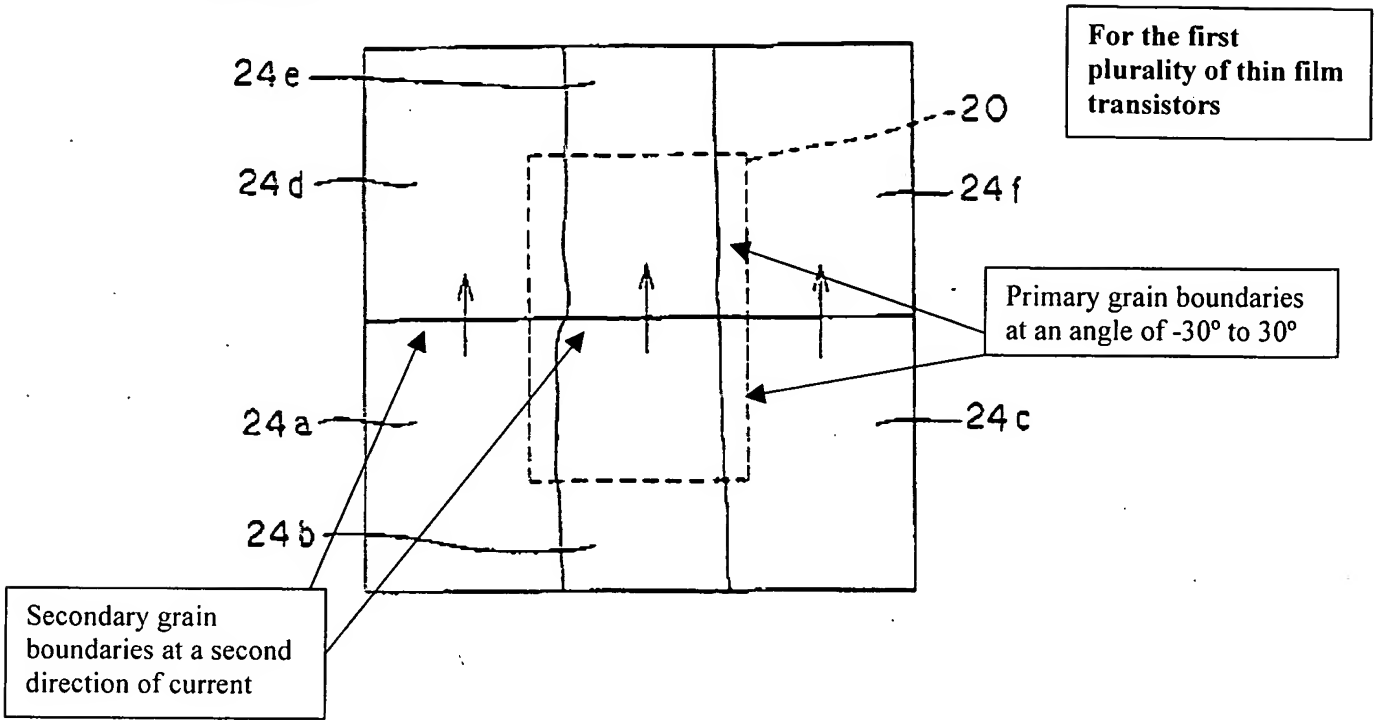
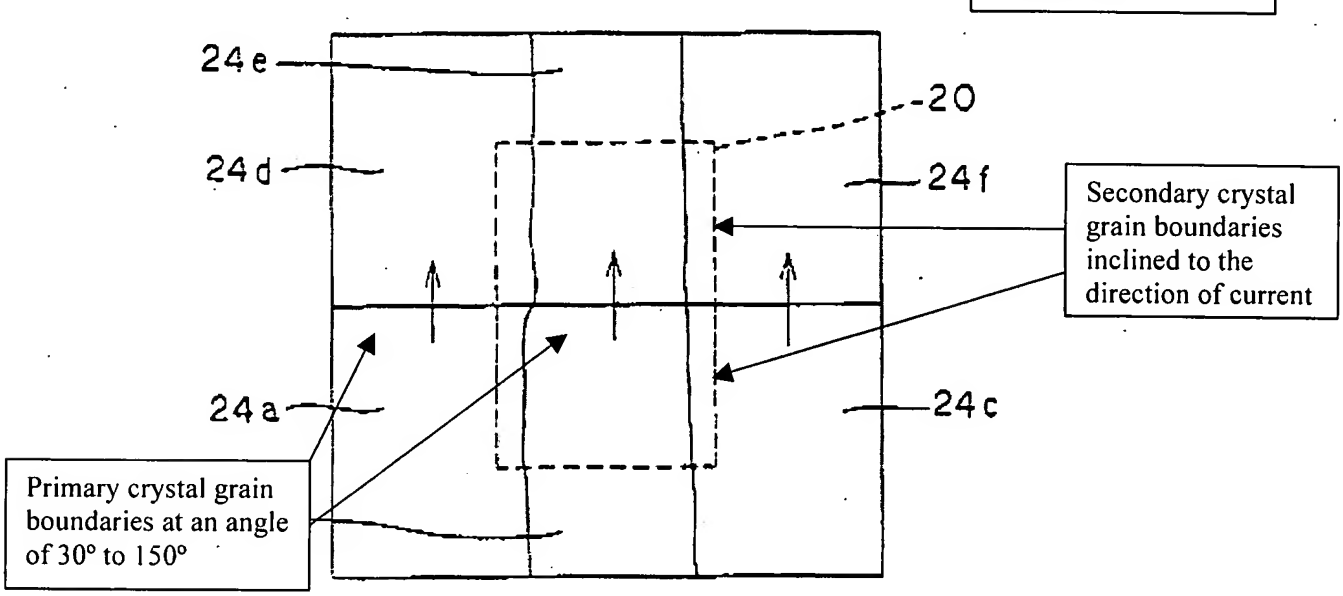

24e
20
24d
24f
Primary grain boundaries at an angle of -30° to 30°
24a
24c
24b
Secondary grain boundaries at a second direction of current
For the first plurality of thin film transistors

FIG.44


For the second plurality of thin film transistors
24e
20
24d
24f
Secondary crystal grain boundaries inclined to the direction of current
24a
24c
Primary crystal grain boundaries at an angle of 30° to 150°

Applicant's claimed material does not provide unexpected results that are not within the teaching applied, since both grain boundaries disclosed in Mitanaga and Shimizu as well as the grain boundaries disclose by the Applicant perform the same function of improving the electrical characteristics of the polysilicon film. Thus, it would have been obvious at the time of the invention to one of ordinary skill in the art to combine the polysilicon film of Mitanaga et al ('997) with the secondary crystal grain boundary orientations as taught by Shimizu et al ('146). Motivation to combine would be to improve the electrical characteristics of the polysilicon film.

In regard to claim 2, Mitanaga et al ('997) teach the primary crystal grain boundaries (216) are parallel to the first direction of current (column 14 lines 48-55).

In regard to claim 3, Mitanaga et al ('997) teaches a first number of the primary crystal grain boundaries exist in active channel regions of each of the first plurality of thin film transistors (column 13 line 66 to column 14 line 12).

In regard to claim 4, Mitanaga/Shimizu disclose all the limitations set forth, as described above, except the display device is an OLED. The Applicant, however, states that using TFTs in organic electroluminescent displays is known in the art in paragraph 9. The MPEP states that "[w]here the specification identifies work done by another as "prior art," the subject matter so identified is treated as admitted prior art. In re Nomiya, 509 F.2d 566, 571, 184 USPQ 607, 611 (CCPA 1975). Thus, it would have been obvious at the time of the invention to one of ordinary skill in the art to use the polysilicon substrate of Mitanaga/Shimizu in and OLED. Motivation for combining would be to fabricate an active matrix display.

In regard to claim 5, the Applicant is claiming a display device including a method (i.e.: process) of making the polysilicon substrate; consequently, claim 5 is considered a "product-by-process" claim. In spite of the fact that a product-by-process claim may recite only process limitations, it is the product and not the recited process that is coved by the claim. Further, patentability of a claim to a product does not rest merely on the difference in the method by which the product is made. Rather, it is the product itself, which must be new and not obvious (see MPEP 2113). Hence, Mitanaga et al ('997) disclose of a polysilicon substrate meets the structural limitation of the claimed invention.

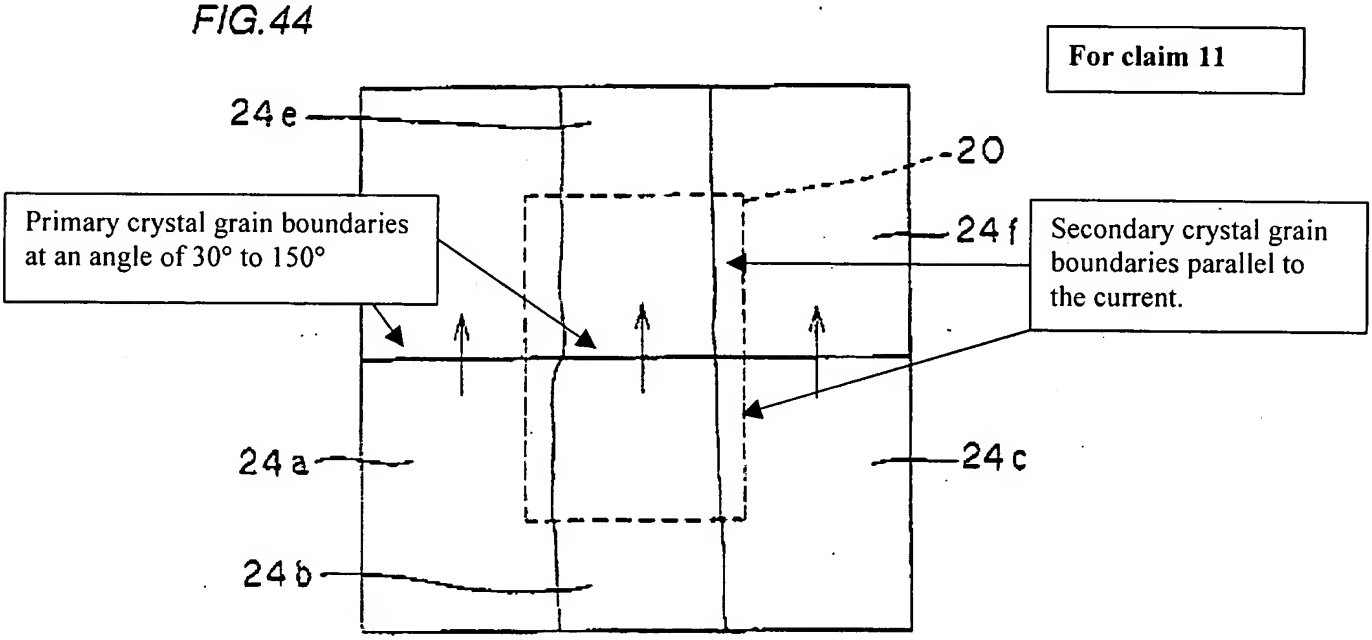
In regard to claim 7, Mitanaga et al ('997) teach the primary crystal grain boundaries are perpendicular to the second direction of current (column 15 line 48-column 16 line 18).

In regard to claim 8, Mitanaga et al ('997) teach second number of the primary crystal grain boundaries exist in active channel regions of each of the second plurality of thin film transistors (column 15 line 48-column 16 line 18).

In regard to claim 11, Mitanaga et al ('997) teach a display device with a polysilicon substrate comprising: a driving region (claim 13); a plurality of thin film transistors in the driving region (claim 10); and primary crystal grain boundaries in the polysilicon substrate in the driving region (claim 10); and secondary primary crystal grain boundaries in the polysilicon substrate in the driving region (claim 10). Mitanaga et al are silent regarding the limitations of wherein the primary crystal grain boundaries are inclined to a direction of current flowing from source to drain of each of the plurality of thin film transistors at an angle of 30° to 150° and the secondary crystal grain boundaries are substantially parallel

to the current flowing from the source to the drain. However, one skilled in the art would reasonably contemplate modifying the device of Mitanaga et al ('997) to include the claimed crystal grain boundaries orientations as an obvious matter of design engineering as evidenced by Shimizu et al ('146). Shimizu et al teach crystal grain boundaries perpendicular to other crystal grain boundaries in many different ways, and Shimizu does not make a distinction between primary and secondary boundaries (column 1 lines 21-42; column 12 line 35 to column 13 line 4). Therefore figure 44 as described below teaches the claimed boundary orientations (arrows indicate current flow).

FIG.44

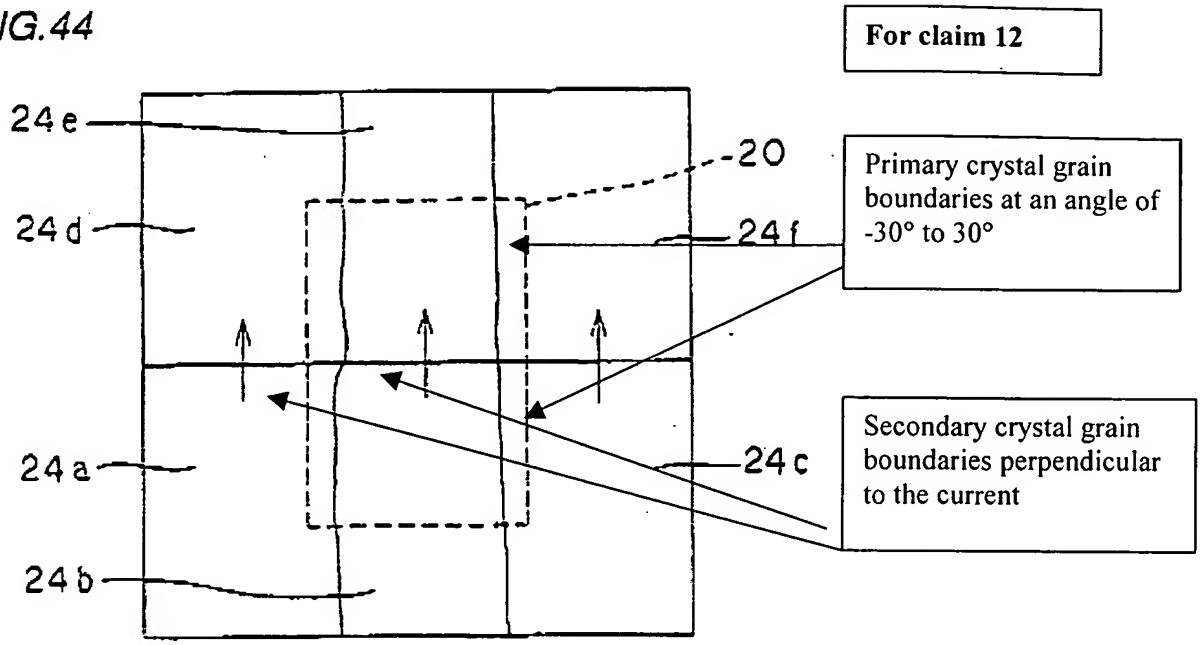


Applicant's claimed material does not provide unexpected results that are not within the teaching applied, since both grain boundaries disclosed in Mitanaga and Shimizu as well as the grain boundaries disclose by the Applicant perform the same function of improving the electrical characteristics of the polysilicon film. Thus, it would have been obvious at the time of the invention to one of ordinary skill in

the art to combine the polysilicon film of Mitanaga et al ('997) with the crystal grain boundary orientations as taught by Shimizu et al ('146). Motivation to combine would be to improve the electrical characteristics of the polysilicon film.

In regard to claim 12, Mitanaga et al ('997) teach a display device with a polysilicon substrate comprising: a display region (claim 14); a plurality of thin film transistors in the display region (claim 10); and primary crystal grain boundaries in the polysilicon substrate in the display region (claim 10); and secondary primary crystal grain boundaries in the polysilicon substrate in the display region (claim 10). Mitanaga et al are silent regarding the limitations of wherein the primary crystal grain boundaries are inclined to a direction of current flowing from source to drain of each of the plurality of thin film transistors at an angle of -30° to 30° and the secondary crystal grain boundaries are substantially perpendicular to the current flowing from the source to the drain. However, one skilled in the art would reasonably contemplate modifying the device of Mitanaga et al ('997) to include the claimed crystal grain boundaries orientations as an obvious matter of design engineering as evidenced by Shimizu et al ('146). Shimizu et al teach crystal grain boundaries perpendicular to other crystal grain boundaries in many different ways, and Shimizu does not make a distinction between primary and secondary boundaries (column 1 lines 21-42; column 12 line 35 to column 13 line 4). Therefore figure 44 as described below teaches the claimed boundary orientations (arrows indicate current flow).

FIG.44



Applicant's claimed material does not provide unexpected results that are not within the teaching applied, since both grain boundaries disclosed in Mitanaga and Shimizu as well as the grain boundaries disclose by the Applicant perform the same function of improving the electrical characteristics of the polysilicon film. Thus, it would have been obvious at the time of the invention to one of ordinary skill in the art to combine the polysilicon film of Mitanaga et al ('997) with the crystal grain boundary orientations as taught by Shimizu et al ('146). Motivation to combine would be to improve the electrical characteristics of the polysilicon film.

Response to Arguments

Applicant's arguments filed 1/17/06 have been fully considered but they are not persuasive.

In regard to Applicant's argument that the prior art of record fails to teach primary and secondary crystal grain boundaries in both the display region and in the driving region of the polysilicon substrate,

the Examiner respectfully disagrees. Mitanaga et al ('997) teaches primary and secondary crystal grain boundaries in both the display region and in the driving region of the polysilicon substrate as described in claims 10, 13, and 14. Therefore, the prior art of record teaches all the limitations in the current application.

In regard to Applicant's argument that the prior art of record fails to teach primary crystal grain boundaries inclined in a first direction of current flowing from source to drain of each of the first plurality of thin film transistors at an angle of 30° to 30° and the secondary crystal grain boundaries are inclined to a second direction of current flowing from source to drain of each of the first plurality of thin film transistors, the Examiner respectfully disagrees. Shimizu et al ('146) teach primary crystal grain boundaries inclined in a first direction of current flowing from source to drain of each of the first plurality of thin film transistors at an angle of 30° to 30° and the secondary crystal grain boundaries are inclined to a second direction of current flowing from source to drain of each of the first plurality of thin film transistors in figure 44. Therefore, the prior art of record teaches all the limitations in the current application.

In regard to Applicant's argument that the prior art of record fails to teach primary crystal grain boundaries are inclined to a second direction of current flowing from source to drain of each of the second plurality of thin film transistors at and angle of 30° to 150° and the secondary crystal grain boundaries are inclined to the first direction of current, the Examiner respectfully disagrees. Shimizu et al ('146) teach primary crystal grain boundaries are inclined to a second direction of current flowing from source to drain of each of the second plurality of thin film transistors at and angle of 30° to 150° and the secondary crystal grain boundaries are inclined to the first direction of current in figure 44. Therefore, the prior art of record teaches all the limitations in the current application.

In regard to Applicant's argument that Mitanaga only teaches the grain boundaries in the two regions of the polysilicon substrate, the Examiner respectfully disagrees. In claim 10, Mitanaga teaches each TFT has a plurality of grain boundaries. The first region grain boundaries extending in a direction parallel with the current, the second region grain boundaries extending in a direction perpendicular to the current . Therefore, the prior art of record teaches all the limitations in the current application.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elizabeth A. Rielley whose telephone number is 571-272-2117. The examiner can normally be reached on Monday - Friday 7:30 - 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar Patel can be reached on 571-272-2457. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Elizabeth Rielley

Examiner
Art Unit 2879

4/13/06
MARICELI SANTIAGO
PRIMARY EXAMINER